

IN THE SPECIFICATION

Page 1, before the first line, add the paragraph:

This is a continuation application of application Serial No. 09/983,373, filed October 24, 2001, which is continuation application of Serial No. 09/690,998, filed October 18, 2000; which is a continuation application of U.S. Serial No. 09/518,696, filed March 3, 2000, now U.S. Patent No. 6,195,719; which is a continuation application of U.S. Serial No. 09/375,356, filed August 17, 1999, now U.S. Patent No. 6,098,136; which is a continuation application of U.S. Serial No. 09/276,968 filed on March 26, 1999, now U.S. Patent No. 6,006,302; which is a continuation application of U.S. Serial No. 09/143,985, filed August 31, 1998; which is a continuation application of U.S. Serial No. 08/959,913, filed October 29, 1997; which is a continuation application of U.S. Serial No. 08/601,993, filed February 15, 1996, now U.S. Patent No. 5,751,976; which is a continuation application of U.S. Serial No. 08/449,088, filed May 24, 1995, now U.S. Patent No. 5,668,956; which is a continuation application of U.S. Serial No. 08/311,893, filed September 26, 1994, now U.S. Patent No. 5,483,642; which is a continuation application of U.S. Serial No. 07/705,701, filed May 23, 1991, now abandoned.

Page 16, the second full paragraph (lines 16-26), replace the paragraph with:

On the other hand, the bus-memory connection controller 401 is connected to the processor address bus 411, the processor control bus 412, the system address bus 417, and the system control bus 418 so as to monitor states of the processor bus 111 and the system bus 113. Moreover, the bus-memory connection controller 401 produces signals for the memory address bus 414 and the memory control bus 415 and the data path control signal 420 to control the main memory 104 and the data path switch 402. The data pass control signal 420 will be described later in detail.

Pages 16 and 17, the paragraph bridging these pages from page 16, line 27 to page 17, line 21, replace the bridging paragraph with:

The bus-memory connection controller 401 causes, in response to a request issued from the processor bus 111 for a processor/main memory access, the processor bus 111 and the memory bus 112 to achieve a cooperative action and then sets the system bus 113 to an independent operation. Furthermore, when a DMA operation request is issued from the system bus 113, the bus-memory connection controller 401 activates the system bus 113 and the memory bus 112 to conduct a cooperative

operation and causes the processor bus 111 to achieve an independent operation. In addition, when the processor bus 111 sends an access request to the system bus 113 or when the system bus 113 issues an access request to the processor bus 111, the bus-memory connection controller 401 sets the processor bus 111 and the system bus 113 in a cooperative action. Moreover, when there appears a conflict between a request from the processor bus 111 and a request from the system bus 113, for example, when memory accesses are simultaneously received therefrom, the bus-memory connection controller 401 develops a function achieving an arbitration control, for example, to set either one of the buses 111 and 113 to a wait state.

Page 18, the first full paragraph (lines 8-24), replace the paragraph with:

The data latches 501, 502, and 503 are disposed to store therein input data respectively from the processor data bus 413, the memory data bus 416, and the system data bus 419. The selectors 504 to 506 are used to select, from input data from the two remaining data buses, data to be respectively supplied to the processor data bus 413, the memory data bus 416, and the system data bus 419, thereby achieving a control operation as follows. Namely, input data of an arbitrary one

of three kinds of data buses is outputted to the buses of other kinds; alternatively, the input data is passed only to one of the other buses. In consequence, based on the data pass control signal 420, all of the three kinds of data buses may be operated in a cooperative manner or a cooperative operation of two arbitrary kinds of buses and an independent operation of the other one kind of bus may be achieved.

Page 20, the first full paragraph (lines 6-16), replace the paragraph with:

The code information created from the sequencer 613 is decoded by the decoder circuit 614, which generates output enable signals 618 to 621 respectively to the I/O drivers 601 to 604, a select signal 622 to the selector circuit 615, a memory control code 623 and a data path control code 624 respectively to the memory control signal generator 616 and the data path control signal generator 617, and control output signals 625 and 626 to be respectively sent to the processor control bus 412 and the system control bus 418 via the I/O drivers 602 and 604, respectively.

Pages 26 and 27, the paragraph bridging these pages from page 26, line 18 to page 27, line 6, replace the paragraph with:

In addition, the latch circuits 501 to 502 of the data path switch 402 shown in Fig. 5 are constituted with edge trigger flip-flops i.e. the latch operation of each latch circuit is initiated at a rising edge of a clock signal (CLK) of Figs. 17 and 18. In this connection, a start signal (START (1901)) is a transfer start signal, namely, while the start signal is being outputted, an address is latched at a rising edge of the clock (CLK), the address being employed in a subsequent operation. Moreover, a signal M_ADD denotes a memory address to be sent to the memory address bus 414, wherein signals P_Data, M_Data, and S_Data indicate data passed to the processor data bus 413, the memory data bus 416, and the system data bus 419, respectively. Furthermore, signals P_Latch, M_Latch, and S_Latch designate data loaded in the latch circuits 501, 502, and 503, respectively.